

# ITS4100S-SJ-N

Smart High-Side NMOS-Power Switch

## Data Sheet

Rev 1.0, 2012-09-01

Standard Power



## 1 Overview

### Features

- CMOS compatible input
- Switching all types of resistive, inductive and capacitive loads
- Fast demagnetization of inductive loads
- Very low standby current
- Optimized Electromagnetic Compatibility (EMC)
- Overload protection
- Current limitation
- Short circuit protection
- Thermal shutdown with restart
- Overvoltage protection (including load dump)
- Reverse battery protection with external resistor
- Loss of GND and loss of V<sub>bb</sub> protection
- Electrostatic Discharge Protection (ESD)
- Green Product (RoHS compliant)

ITS4100S-SJ-N is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications.

### Description

The ITS4100S-SJ-N is a protected single channel Smart High-Side NMOS-Power Switch in a PG-DSO-8 package with charge pump and CMOS compatible input. The device is monolithically integrated in Smart technology.

### Product Summary

Overvoltage protection  $V_{SAZmin} = 41V$

Operating voltage range:  $5V < V_S < 34V$

On-state resistance  $R_{DS(ON)} = \text{typ } 70m\Omega$

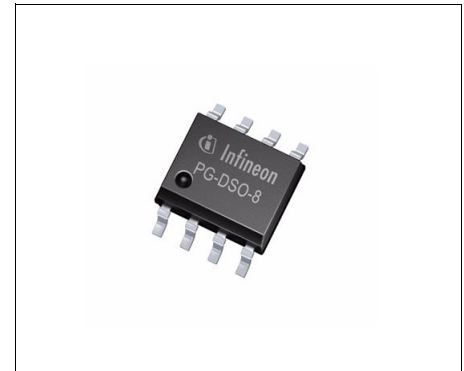
Nominal load current  $I_{LNOM} = 2A$

Operating Temperature range:  $T_j = -40^\circ C$  to  $125^\circ C$

Standby Current:  $I_{SSTB} = 15\mu A$

### Application

- All types of resistive, inductive and capacitive loads
- Power switch for 12V and 24V DC applications with CMOS compatible control interface
- Driver for electromagnetic relays
- Power management for high-side-switching with low current consumption in OFF-mode



PG-DSO-8

Type	Package	Marking
ITS4100S-SJ-N	PG-DSO-8	I100SN

## 2 Block Diagram and Terms

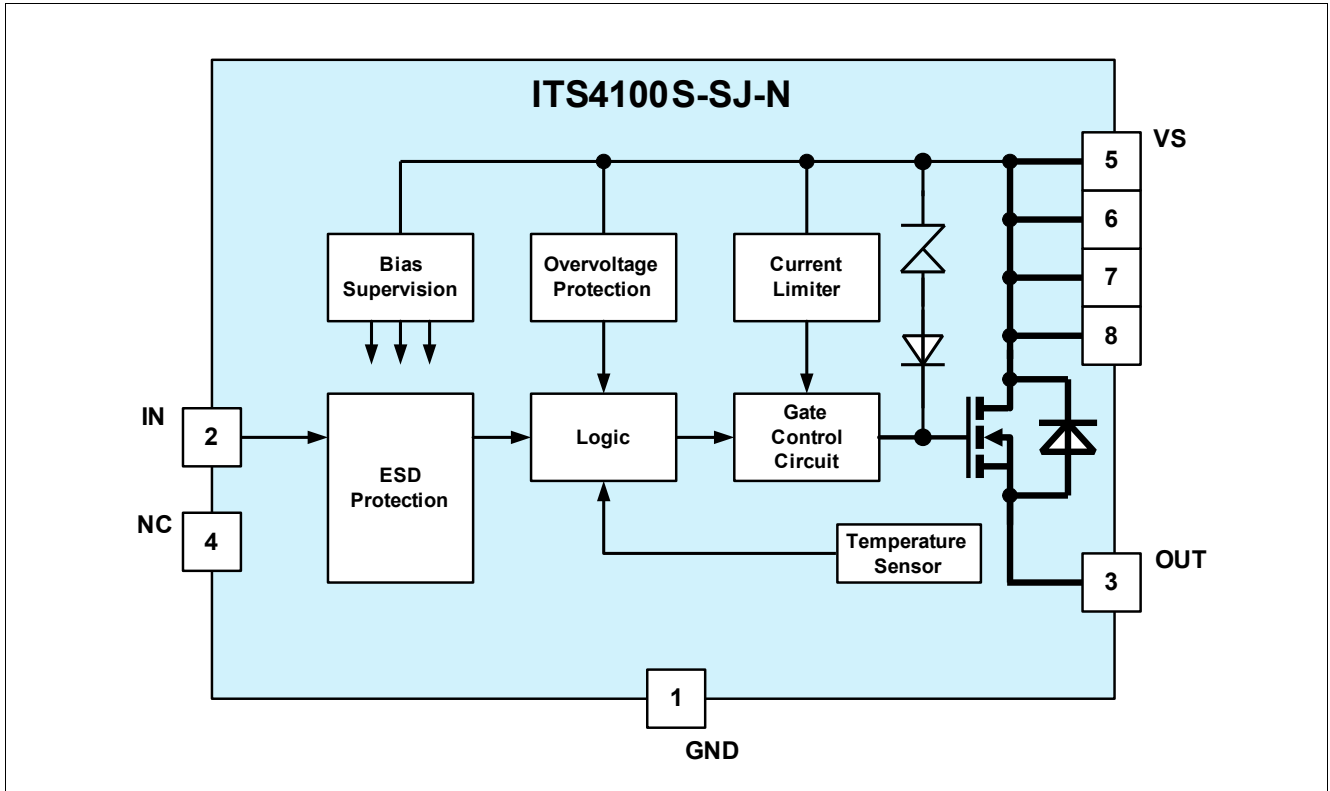


Figure 1 Block diagram

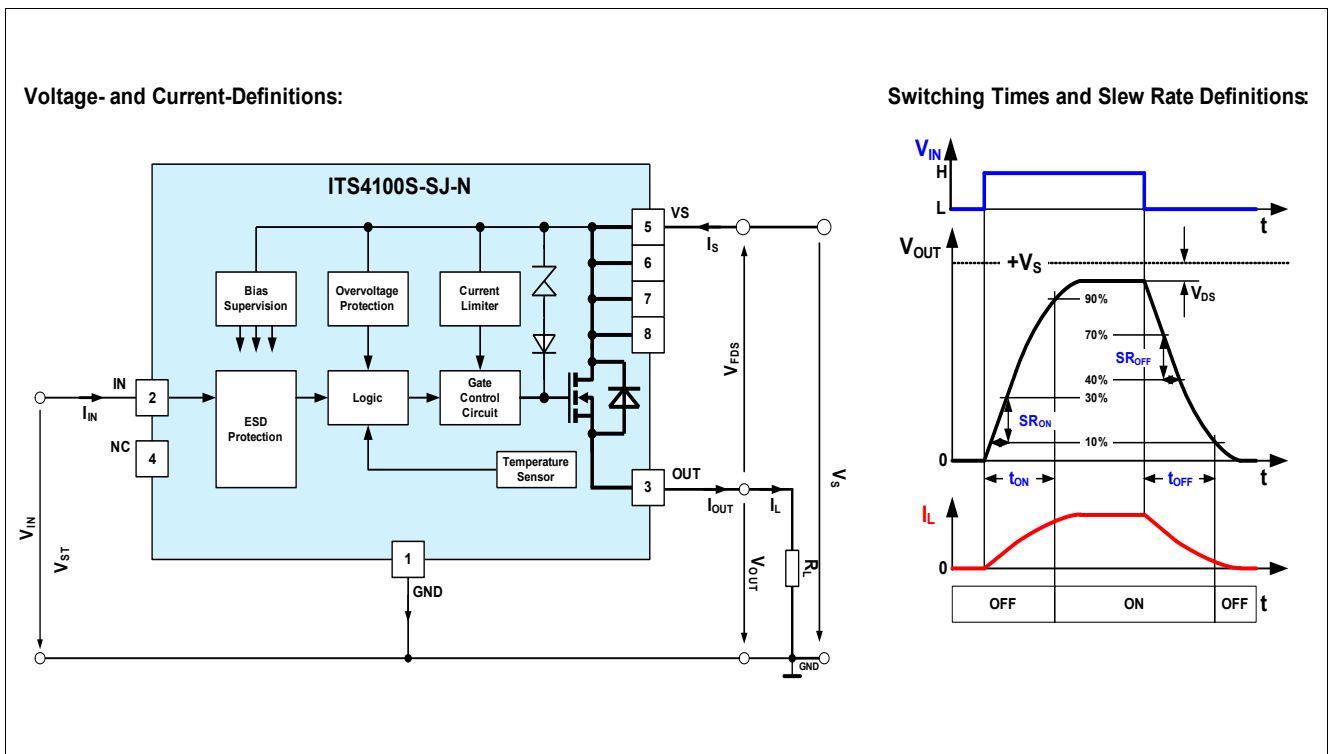


Figure 2 Terms - parameter definition

### 3 Pin Configuration

#### 3.1 Pin Assignment

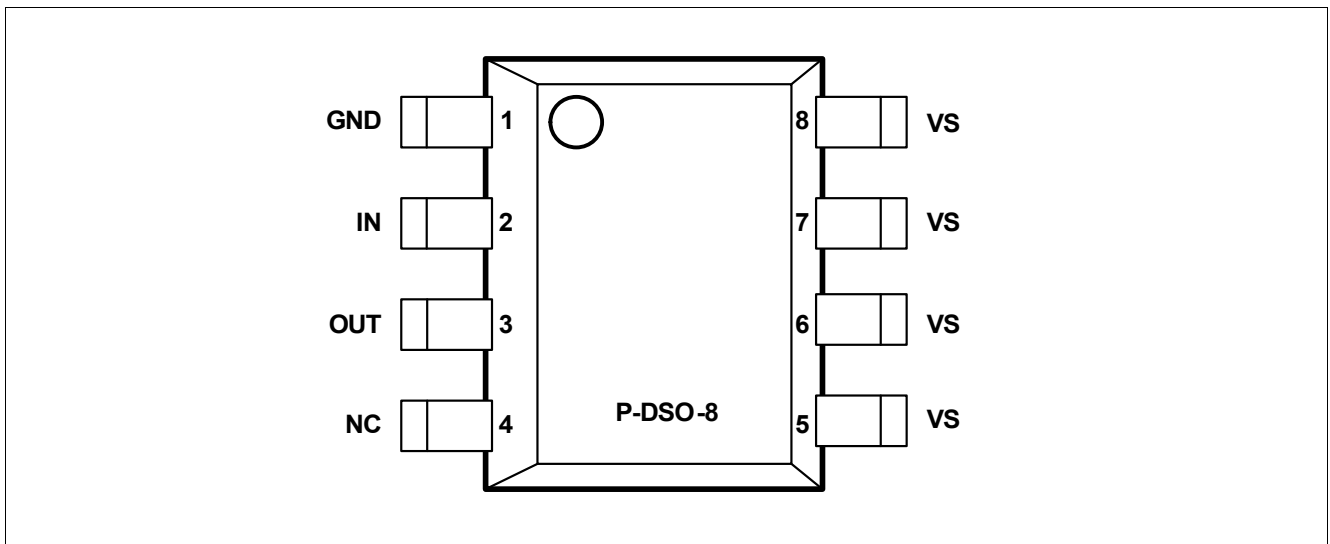


Figure 3 Pin configuration top view, PG-DSO-8

#### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Logic ground
2	IN	Input, controls the power switch; the powerswitch is ON when high
3	OUT	Output to the load
4	NC	Not connected
5, 6, 7, 8	VS	Supply voltage (design the wiring for the maximum short circuit current and also for low thermal resistance)

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute maximum ratings<sup>1)</sup> at  $T_j = 25^\circ\text{C}$  unless otherwise specified. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms"**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Supply voltage VS</b>							
Voltage	$V_S$			40	V		4.1.1
Voltage for short circuit protection	$V_{SSC}$			$V_S$	V	$-40^\circ\text{C} < T_j < 150^\circ\text{C}$	4.1.2
<b>Output stage OUT</b>							
Output Current; (Short circuit current see electrical characteristics)	$I_{OUT}$			self limited	A		4.1.3
<b>Input IN</b>							
Voltage	$V_{IN}$	-10		16	V		4.1.4
Current	$I_{IN}$	-5		5	mA		4.1.5
<b>Temperatures</b>							
Junction Temperature	$T_j$	-40		125	$^\circ\text{C}$		4.1.6
Storage Temperature	$T_{stg}$	-55		125	$^\circ\text{C}$		4.1.7
<b>Power dissipation</b>							
$T_a = 25^\circ\text{C}^{2)}$	$P_{tot}$			1.5	W		4.1.8
<b>Inductive load switch-off energy dissipation</b>							
$T_j = 125^\circ\text{C}; V_S = 13.5\text{V}; I_L = 1\text{A}^{3)}$	$E_{AS}$			870	mJ	single pulse	4.1.9
<b>ESD Susceptibility</b>							
ESD susceptibility (input pin)	$V_{ESD}$	-1		1	kV	HBM <sup>4)</sup>	4.1.10
ESD susceptibility (all other pins)	$V_{ESD}$	-5		5	kV	HBM <sup>4)</sup>	4.1.11

1) Not subject to production test, specified by design

2) Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70mm thick) copper area for V<sub>bb</sub> connection. PCB is vertical without blown air

3) Not subject to production test, specified by design

4) ESD susceptibility HBM according to EIA/JESD 22-A 114.

*Note: Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" the normal operating range. Protection functions are neither designed for continuous nor repetitive operation.*

## 4.2 Functional Range

**Table 2 Functional Range**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Nominal Operating Voltage	$V_S$	5		34	V	$V_S$ increasing	4.2.1

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal Resistance<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance - Junction to pin5	$R_{thj-pin5}$		32.0		K/W		4.3.1
Thermal Resistance - Junction to Ambient - 1s0p, minimal footprint	$R_{thJA\_1s0p}$		135.3		K/W	<sup>2)</sup>	4.3.2
Thermal Resistance - Junction to Ambient - 1s0p, 300mm <sup>2</sup>	$R_{thJA\_1s0p\_300mm^2}$		86.1		K/W	<sup>3)</sup>	4.3.3
Thermal Resistance - Junction to Ambient - 1s0p, 600mm <sup>2</sup>	$R_{thJA\_1s0p\_600mm^2}$		75.3		K/W	<sup>4)</sup>	4.3.4
Thermal Resistance - Junction to Ambient - 2s2p	$R_{thJA\_2s2p}$		66.8		K/W	<sup>5)</sup>	4.3.5
Thermal Resistance - Junction to Ambient with thermal vias - 2s2p	$R_{thJA\_2s2p}$		58.4		K/W	<sup>6)</sup>	4.3.6

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, footprint; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, Cu, 300mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board, 600mm<sup>2</sup>; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 1x 70 $\mu$ m Cu.
- 5) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu).
- 6) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board with two thermal vias; the Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 $\mu$ m Cu, 2 x 35 $\mu$ m Cu). The diameter of the two vias are equal 0.3mm and have a plating of 25 $\mu$ m with a copper heatsink area of 3mm x 2mm). JEDEC51-7: The two plated-through hole vias should have a solder land of no less than 1.25 mm diameter with a drill hole of no less than 0.85 mm diameter.



## 5 Electrical Characteristics

**Table 4**  $V_S=13.5V$ ;  $T_j = -40^{\circ}C$  to  $125^{\circ}C$ ; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at  $V_S = 13.5V$ ,  $T_j = 25^{\circ}C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
<b>Powerstage</b>							
NMOS ON Resistance	$R_{DSON}$		70	100	m $\Omega$	$I_{OUT}= 2A$ ; $T_j = 25^{\circ}C$ ; $9V < V_S < 34V$ ; $V_{IN}= 5V$	5.0.1
NMOS ON Resistance	$R_{DSON}$		140	200	m $\Omega$	$I_{OUT}= 2A$ ; $T_j = 125^{\circ}C$ ; $9V < V_S < 34V$ ; $V_{IN}= 5V$	5.0.2
Nominal Load Current; device on PCB <sup>1)</sup>	$I_{LNOM}$	2.0	2.4		A	$T_{pin5} = 85^{\circ}C$	5.0.3
<b>Timings of Power Stages<sup>2)</sup></b>							
Turn ON Time(to 90% of $V_{out}$ ); L to H transition of $V_{IN}$	$t_{ON}$		90	170	$\mu s$	$V_S=13.5V$ ; $R_L = 47\Omega$	5.0.4
Turn OFF Time (to 10% of $V_{out}$ ); H to L transition of $V_{IN}$	$t_{OFF}$		90	230	$\mu s$	$V_S=13.5V$ ; $R_L = 47\Omega$	5.0.5
ON-Slew Rate (10 to 30% of $V_{out}$ ); L to H transition of $V_{IN}$	$SR_{ON}$		0.8	1.7	V / $\mu s$	$V_S=13.5V$ ; $R_L = 47\Omega$	5.0.6
OFF-Slew Rate; $dV_{OUT} / dt_{ON}$ (70 to 40% of $V_{out}$ ); H to L transition of $V_{IN}$	$SR_{OFF}$		0.8	1.7	V / $\mu s$	$V_S=13.5V$ ; $R_L = 47\Omega$	5.0.7
<b>Under voltage lockout (charge pump start-stop-restart)</b>							
Supply undervoltage; charge pump stop voltage	$V_{SUV}$			5.5	V	$V_S$ decreasing	5.0.8
Supply startup voltage; Charge pump restart voltage	$V_{SSU}$		4.0	5.5	V	$V_S$ increasing	5.0.9
<b>Current consumption</b>							
Operating current	$I_{GND}$		0.5	1.3	mA	$V_{IN}= 5V$	5.0.10
Standby current	$I_{SSTB}$			10	$\mu A$	$V_{IN}= 0V$ ; $V_{OUT}= 0V$ ; $-40^{\circ}C < T_j < 85^{\circ}C$	5.0.11
Standby current	$I_{SSTB}$			15	$\mu A$	$V_{IN}= 0V$ ; $V_{OUT}= 0V$ ; $T_j = 125^{\circ}C$	5.0.12
Output leakage current	$I_{OUTLK}$			5	$\mu A$	$V_{IN}= 0V$ ; $V_{OUT}= 0V$	5.0.13
<b>Protection functions <sup>3)</sup></b>							
Initial peak short circuit current limit	$I_{LSCP}$			18	A	$T_j = -40^{\circ}C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu As$	5.0.14
Initial peak short circuit current limit	$I_{LSCP}$		10		A	$T_j = 25^{\circ}C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu As$	5.0.15

## Electrical Characteristics

**Table 4**  $V_S=13.5V$ ;  $T_j = -40^\circ C$  to  $125^\circ C$ ; all voltages with respect to ground. Currents flowing into the device unless otherwise specified in chapter "Block Diagram and Terms". Typical values at  $V_S = 13.5V$ ,  $T_j = 25^\circ C$

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Initial peak short circuit current limit	$I_{LSCP}$	4			A	$T_j = 125^\circ C$ ; $V_S = 20V$ ; $V_{IN} = 5.0V$ ; $t_m = 150\mu s$	5.0.16
Repetitive short circuit current limit $T_j = T_{jTrip}$ ; see timing diagrams	$I_{LSCR}$		7		A	$V_{IN} = 5.0V$	5.0.17
Output clamp at $V_{OUT} = V_S - V_{DSCL}$ (inductive load switch off)	$V_{DSCL}$	41	47		V	$I_S = 4mA$	5.0.18
Overvoltage protection $V_{OUT} = V_S - V_{ONCL}$	$V_{SAZ}$	41			V	$I_S = 4mA$	5.0.19
Thermal overload trip temperature	$T_{jTrip}$	150			$^\circ C$		5.0.20
Thermal hysteresis	$T_{HYS}$		10		K		5.0.21
<b>Reverse Battery<sup>4)</sup></b>							
Continuous reverse battery voltage	$V_{SREV}$	- 32			V		5.0.22
Forward voltage of the drain-source reverse diode	$V_{FDS}$		600		mV	$I_{FDS} = 200mA$ ; $V_{IN} = 0V$ ; $T_j = 125^\circ C$	5.0.23
<b>Input interface; pin IN</b>							
Input turn-ON threshold voltage	$V_{INON}$	2.2			V		5.0.24
Input turn-OFF threshold voltage	$V_{INOFF}$			0.8	V		5.0.25
Input threshold hysteresis	$V_{INHYS}$		0.3		V		5.0.26
Off state input current	$I_{INOFF}$	1		30	$\mu A$	$V_{IN} = 0.7V$	5.0.27
On state input current	$I_{INON}$	1		30	$\mu A$	$V_{IN} = 5.0V$	5.0.28
Input resistance	$R_{IN}$	1.5	3.5	5.0	k $\Omega$		5.0.29

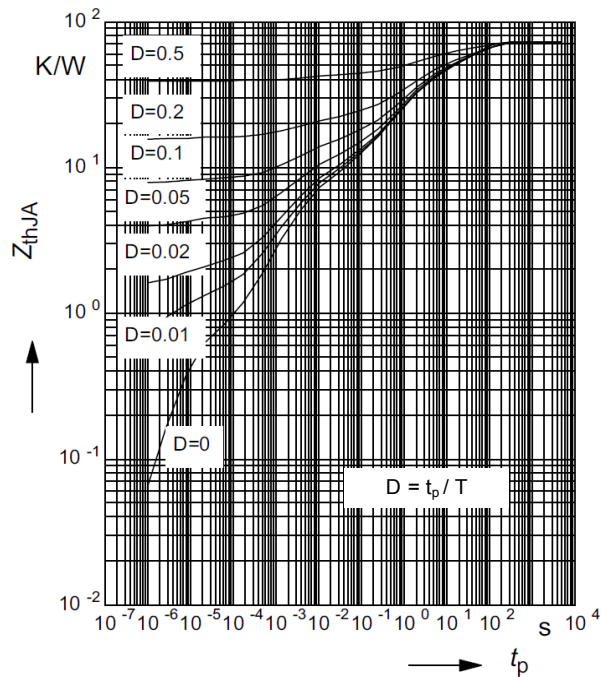
- 1) Device on 50mm x 50mm x 1,5mm epoxy FR4 PCB with 6cm<sup>2</sup> (one layer copper 70um thick) copper area for supply voltage connection. PCB in vertical position without blown air.
- 2) Timing values only with high slewrates input signal; otherwise slower.
- 3) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 4) Requires a 150W resistor in GND connection. The reverse load current through the intrinsic drain-source diode of the power-MOS has to be limited by the connected load. Power dissipation is higher compared to normal operation due to the voltage drop across the drain-source diode. The temperature protection is not functional during reverse current operation! Input current has to be limited (see max ratings).



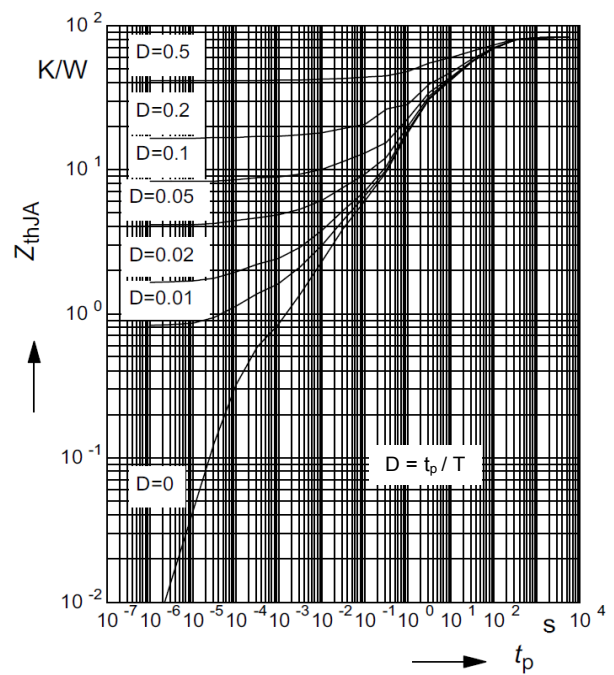
## 6 Typical Performance Graphs

### Typical Performance Characteristics

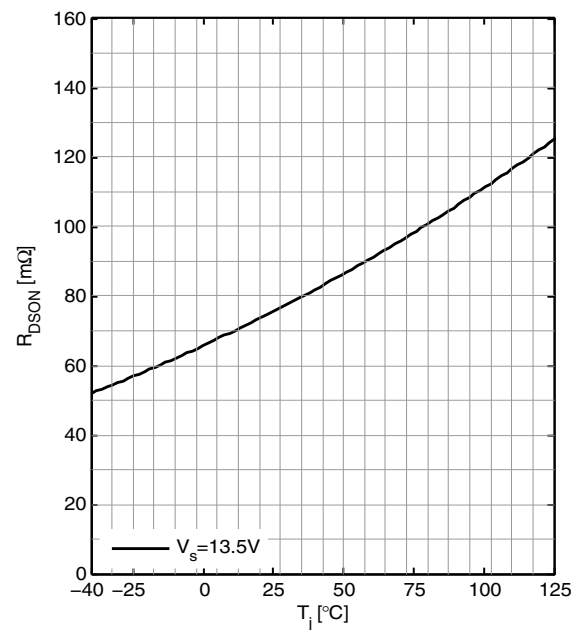
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ 6cm<sup>2</sup> heatsink area



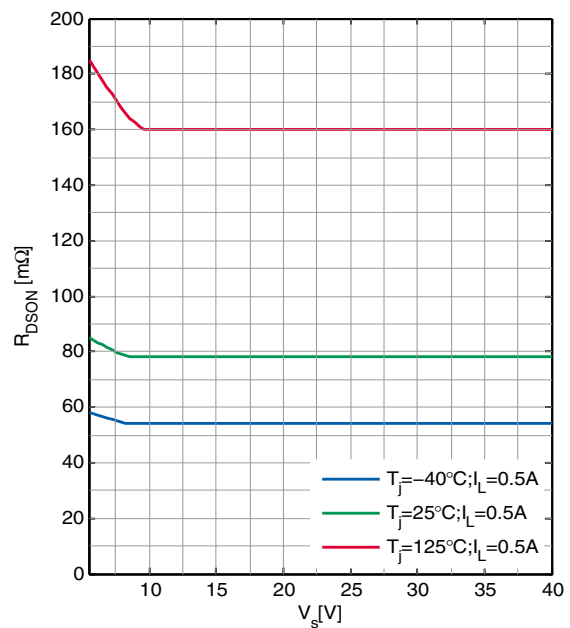
Transient Thermal Impedance  $Z_{thJA}$  versus Pulse Time  $t_p$  @ min footprint



On-Resistance  $R_{DS(on)}$  versus Junction Temperature  $T_j$

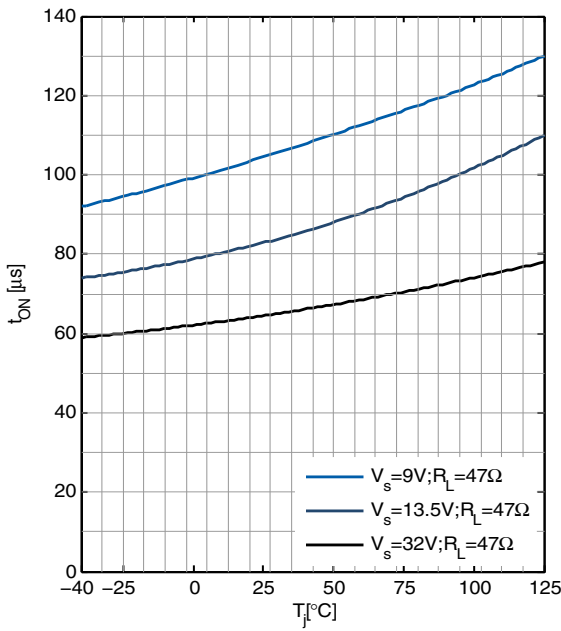


On-Resistance  $R_{DS(on)}$  versus Supply Voltage  $V_s$

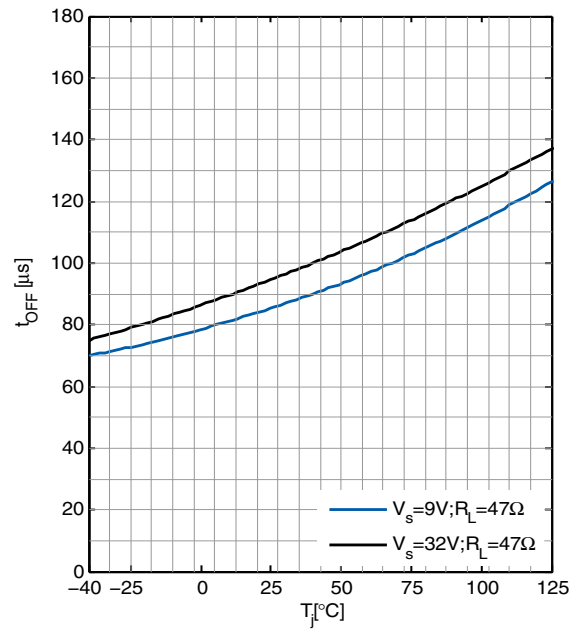


Typical Performance Characteristics

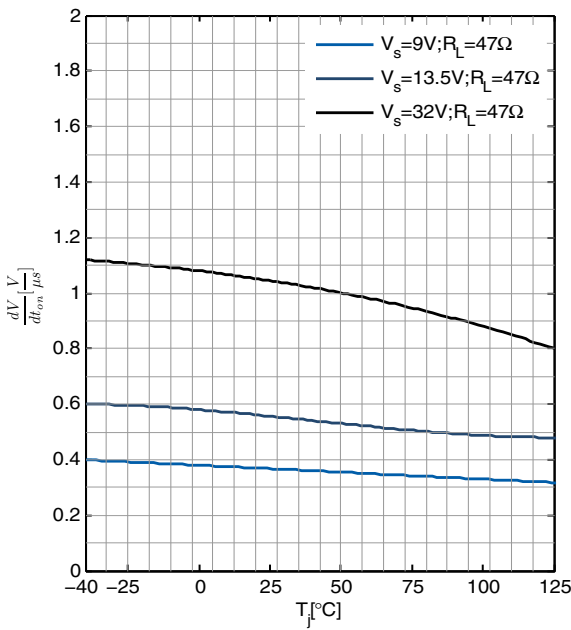
Switch ON Time  $t_{ON}$  versus Junction Temperature  $T_j$



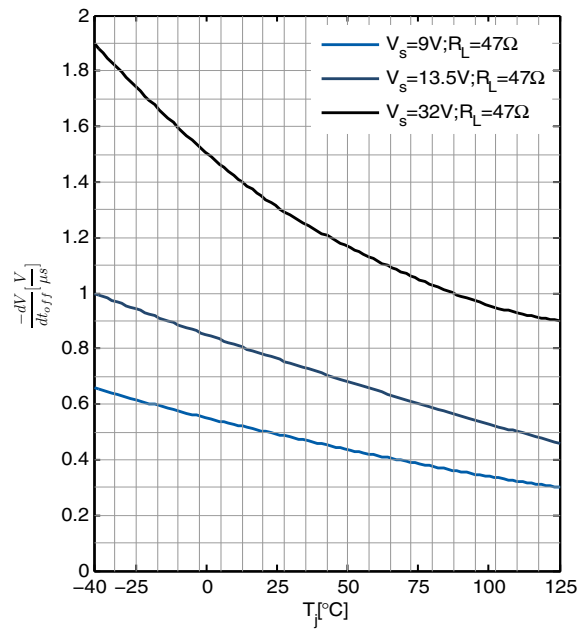
Switch OFF Time  $t_{OFF}$  versus Junction Temperature  $T_j$



ON Slewrate  $SR_{ON}$  versus Junction Temperature  $T_j$

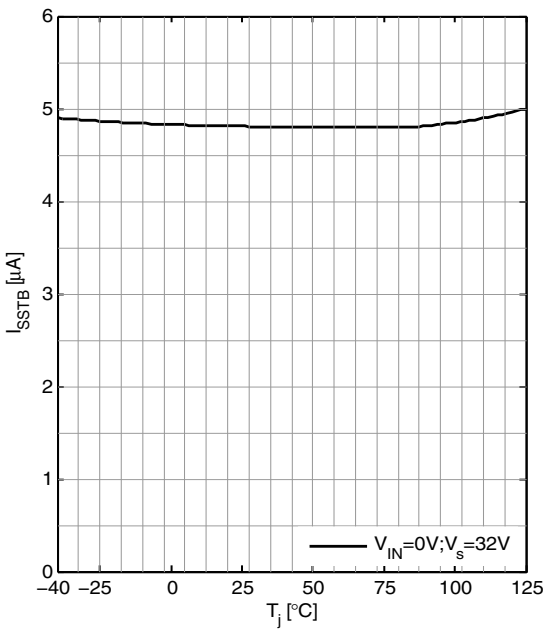


OFF Slewrate  $SR_{OFF}$  versus Junction Temperature  $T_j$

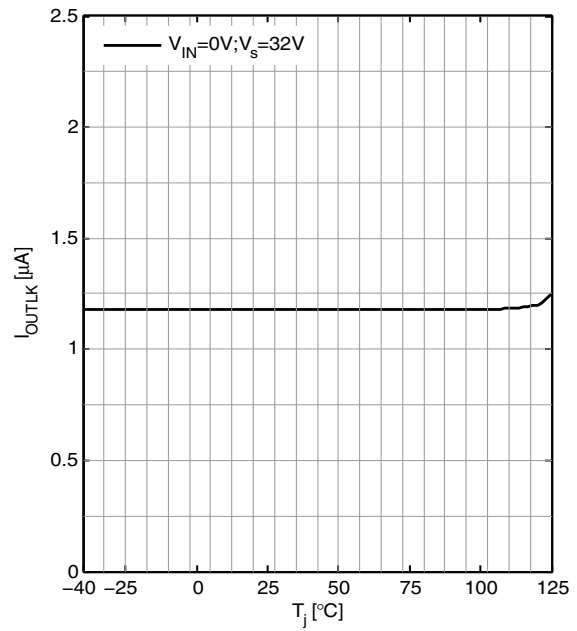


Typical Performance Characteristics

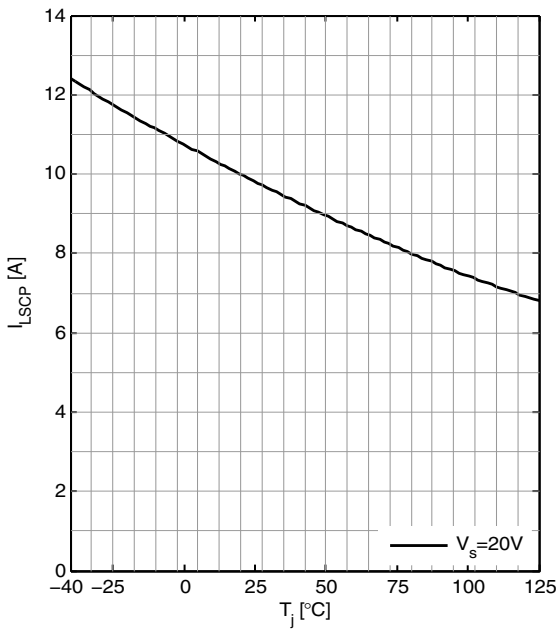
Standby Current  $I_{SSTB}$  versus Junction Temperature  $T_j$



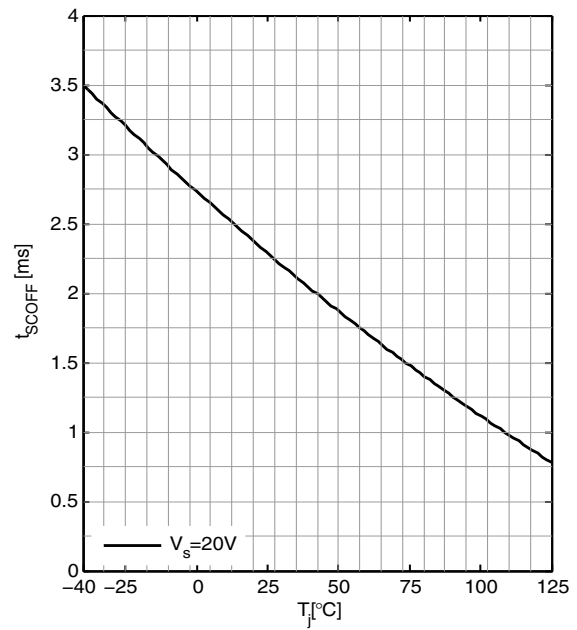
Output Leakage current  $I_{OUTLK}$  versus Junction Temperature  $T_j$



Initial Peak Short Circuit Current Limit  $I_{LSCP}$  versus Junction Temperature  $T_j$

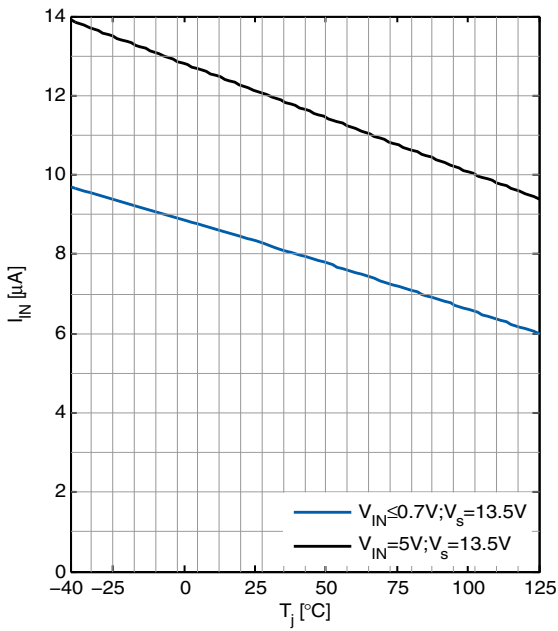


Initial Short Circuit Shutdown time  $t_{SCOFF}$  versus Junction Temperature  $T_j$

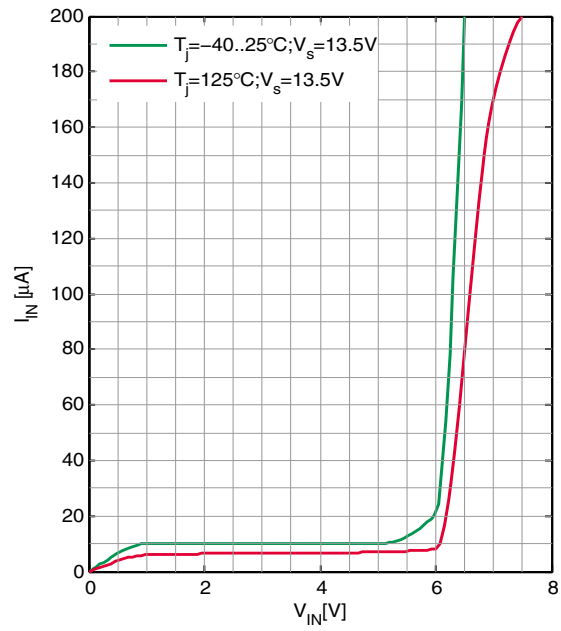


Typical Performance Characteristics

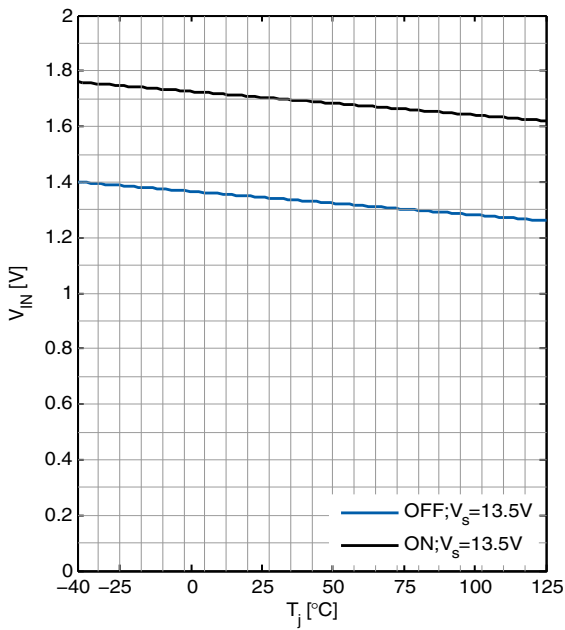
Input Current Consumption  $I_{IN}$  versus Junction Temperature  $T_j$



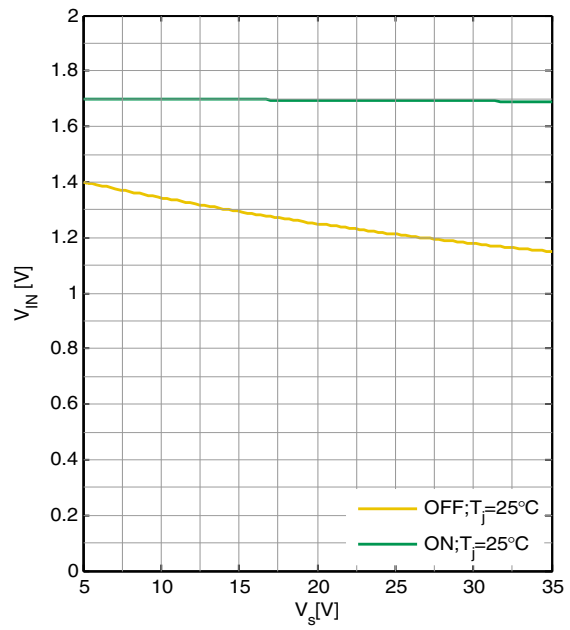
Input Current Consumption  $I_{IN}$  versus Input voltage  $V_{IN}$



Input Threshold voltage  $V_{IN,H,L}$  versus Junction Temperature  $T_j$

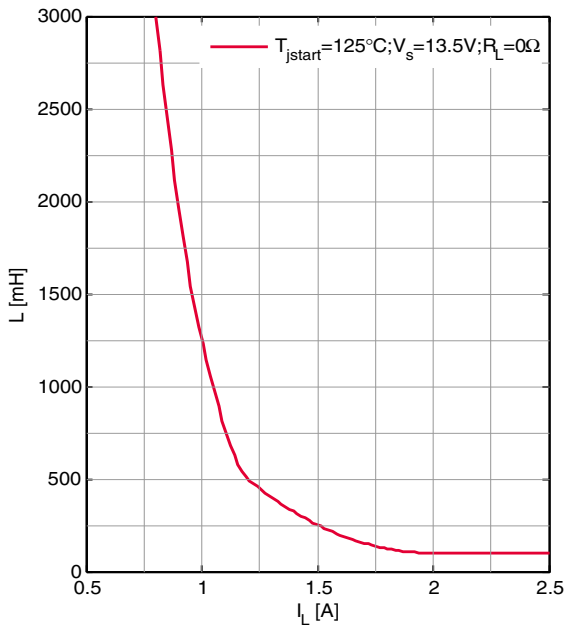


Input Threshold voltage  $V_{IN,H,L}$  versus Supply Voltage  $V_S$

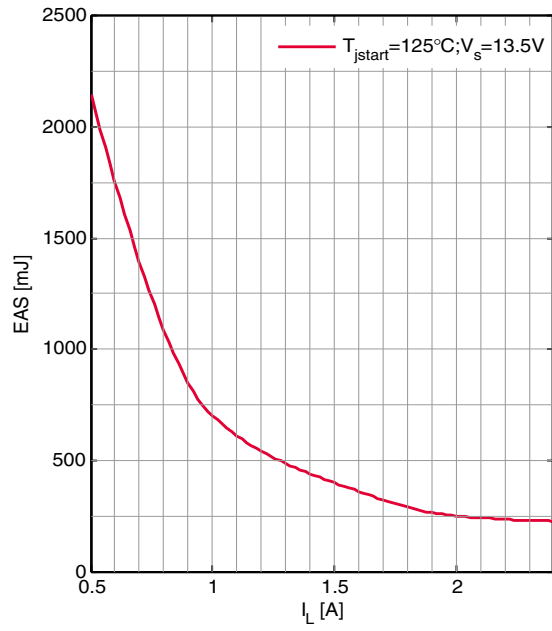


Typical Performance Characteristics

Max. allowable Load Inductance  $L$  versus Load current  $I_L$



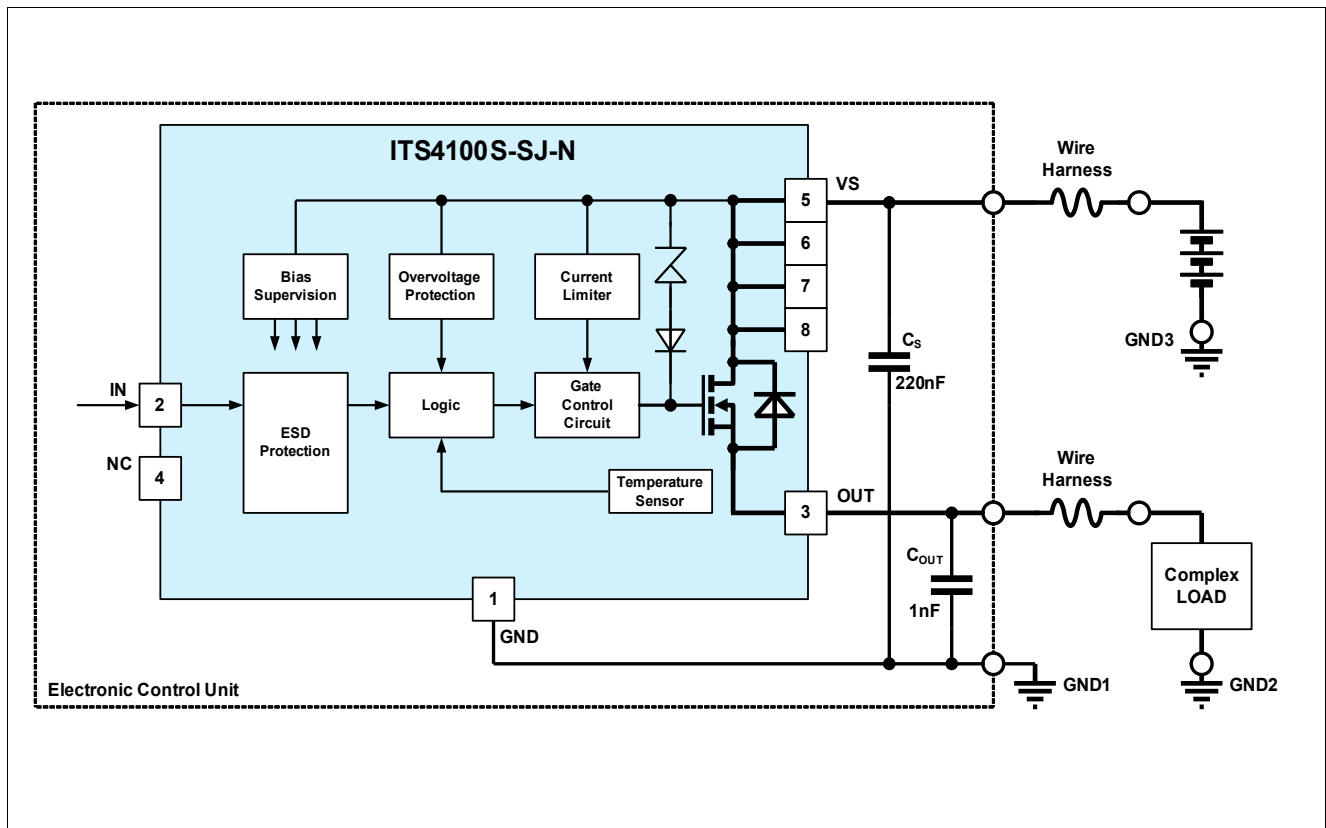
Max. allowable Inductive single pulse Switch-off Energy  $E_{AS}$  versus Load current  $I_L$



## 7 Application Information

### 7.1 Application Diagram

The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty for a certain functionality, condition or quality of the device.



**Figure 4 Application Diagram**

The ITS4100S-SJ-N can be connected directly to a supply network. It is recommended to place a ceramic capacitor (e.g.  $C_S = 220\text{nF}$ ) between supply and GND to avoid line disturbances. Wire harness inductors/resistors are sketched in the application circuit above.

The complex load (resistive, capacitive or inductive) must be connected to the output pin OUT.

A built-in current limit protects the device against destruction.

The ITS4100S-SJ-N can be switched on and off with standard logic ground related logic signal at pin IN.

In standby mode (IN=L) the ITS4100S-SJ-N is deactivated with very low current consumption.

The output voltage slope is controlled during on and off transition to minimize emissions. Only a small ceramic capacitor  $C_{OUT}=1\text{nF}$  is recommended to attenuate RF noise.

In the following chapters the main features, some typical waveforms and the protection behaviour of the ITS4100S-SJ-N is shown. For further details please refer to application notes on the Infineon homepage.

## 7.2 Special Feature Description

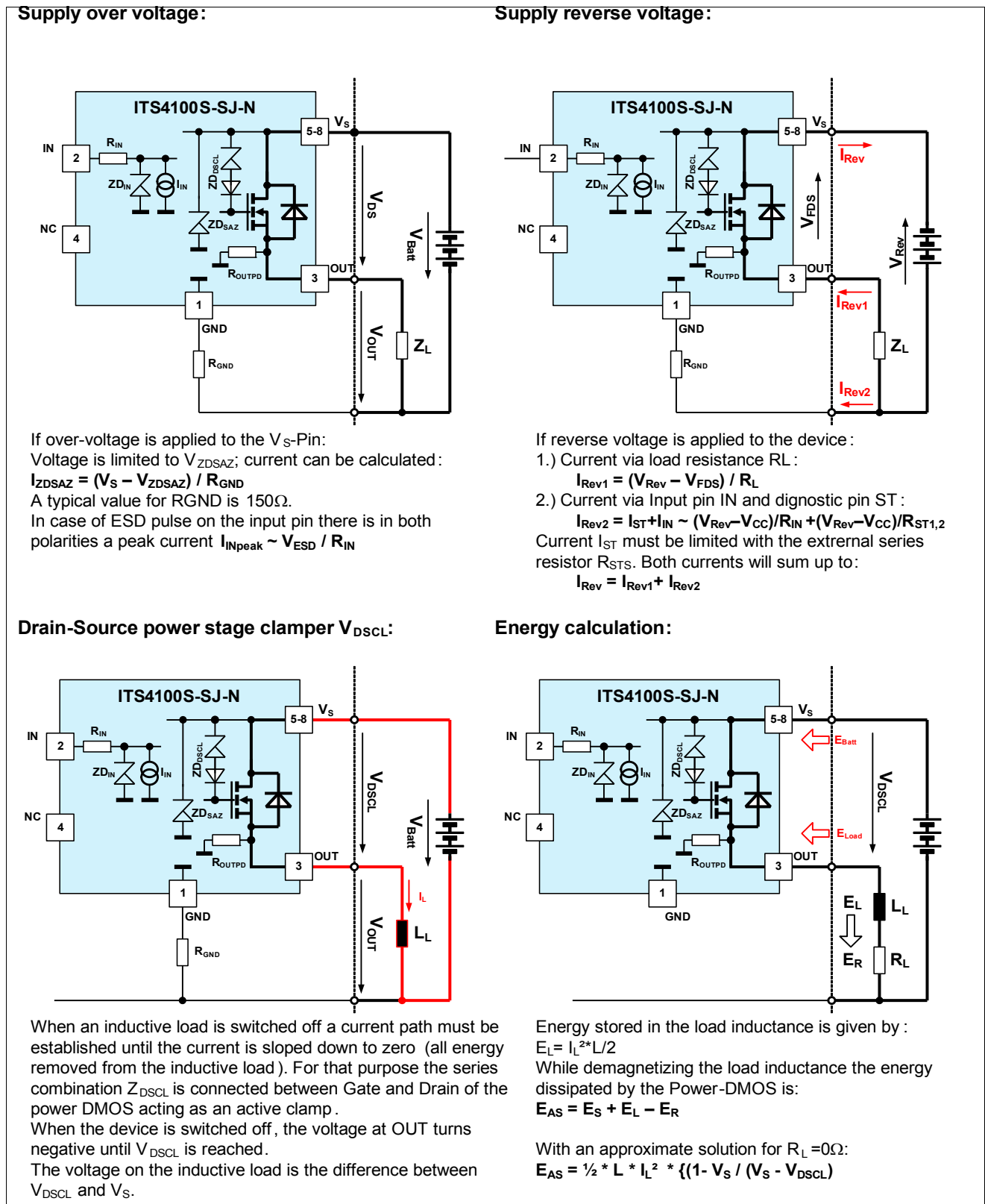


Figure 5 Special feature description



## 7.3 Typical Application Waveforms

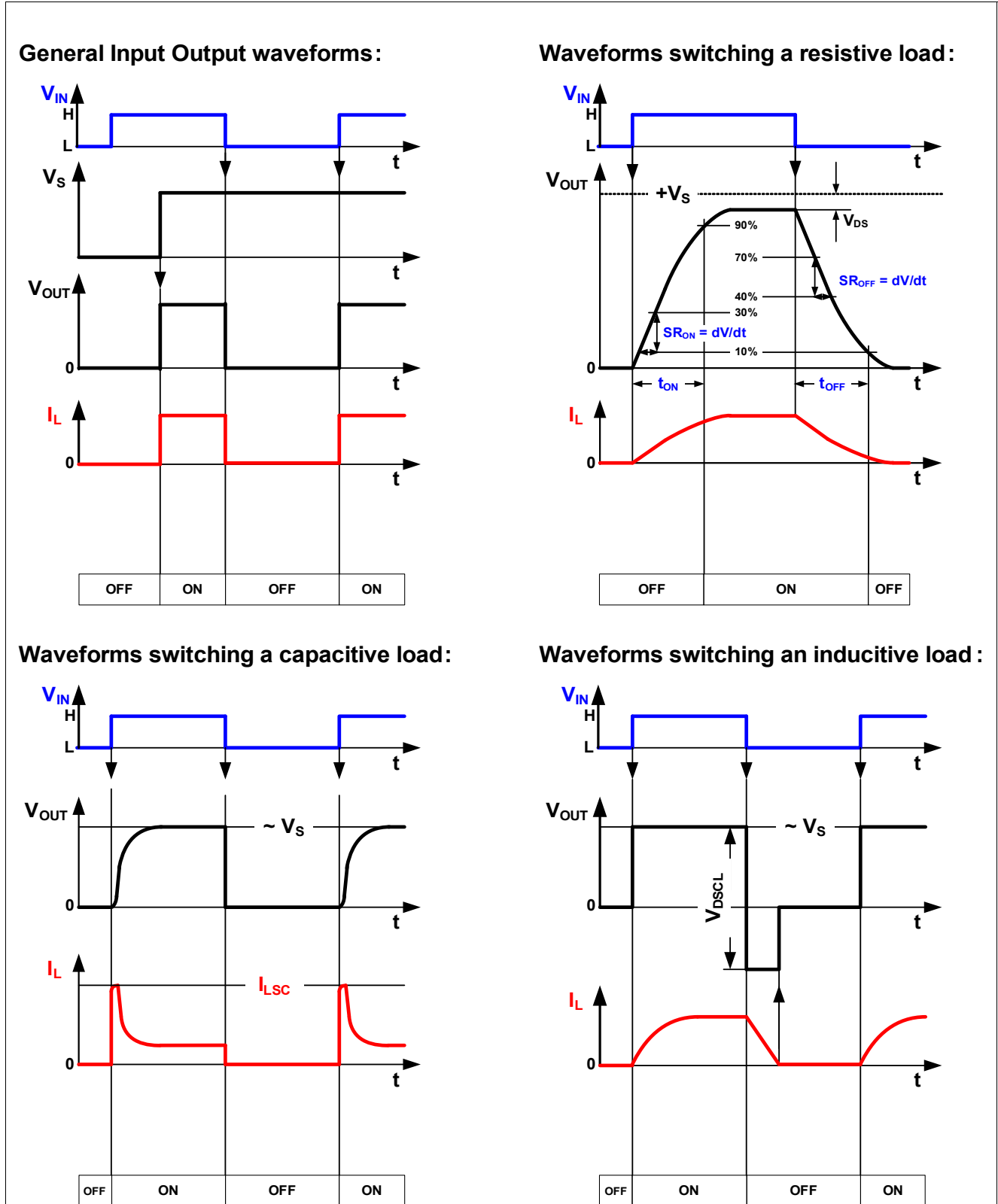


Figure 6 Typical application waveforms of the ITS4100S-SJ-N

## 7.4 Protection Behavior

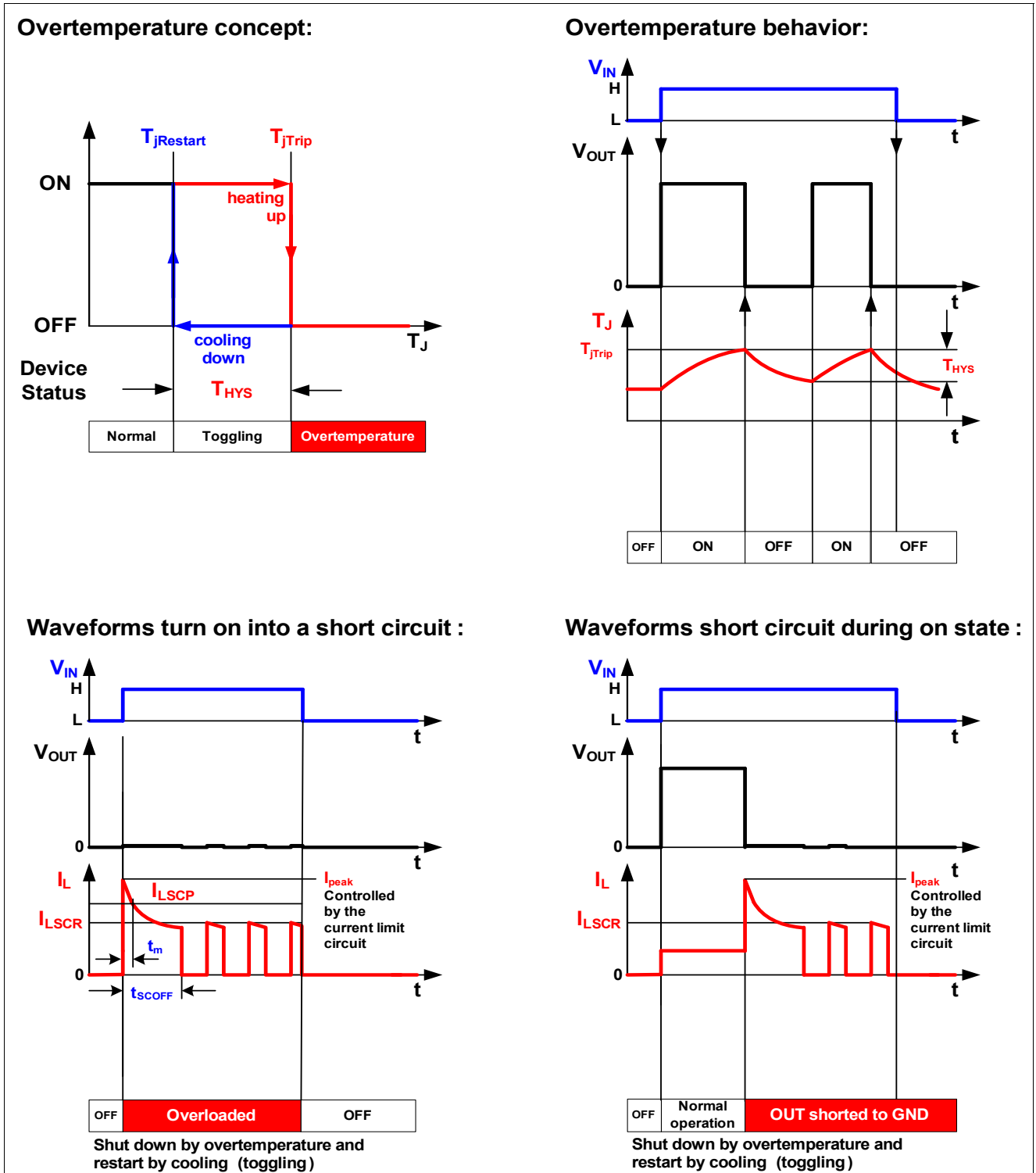
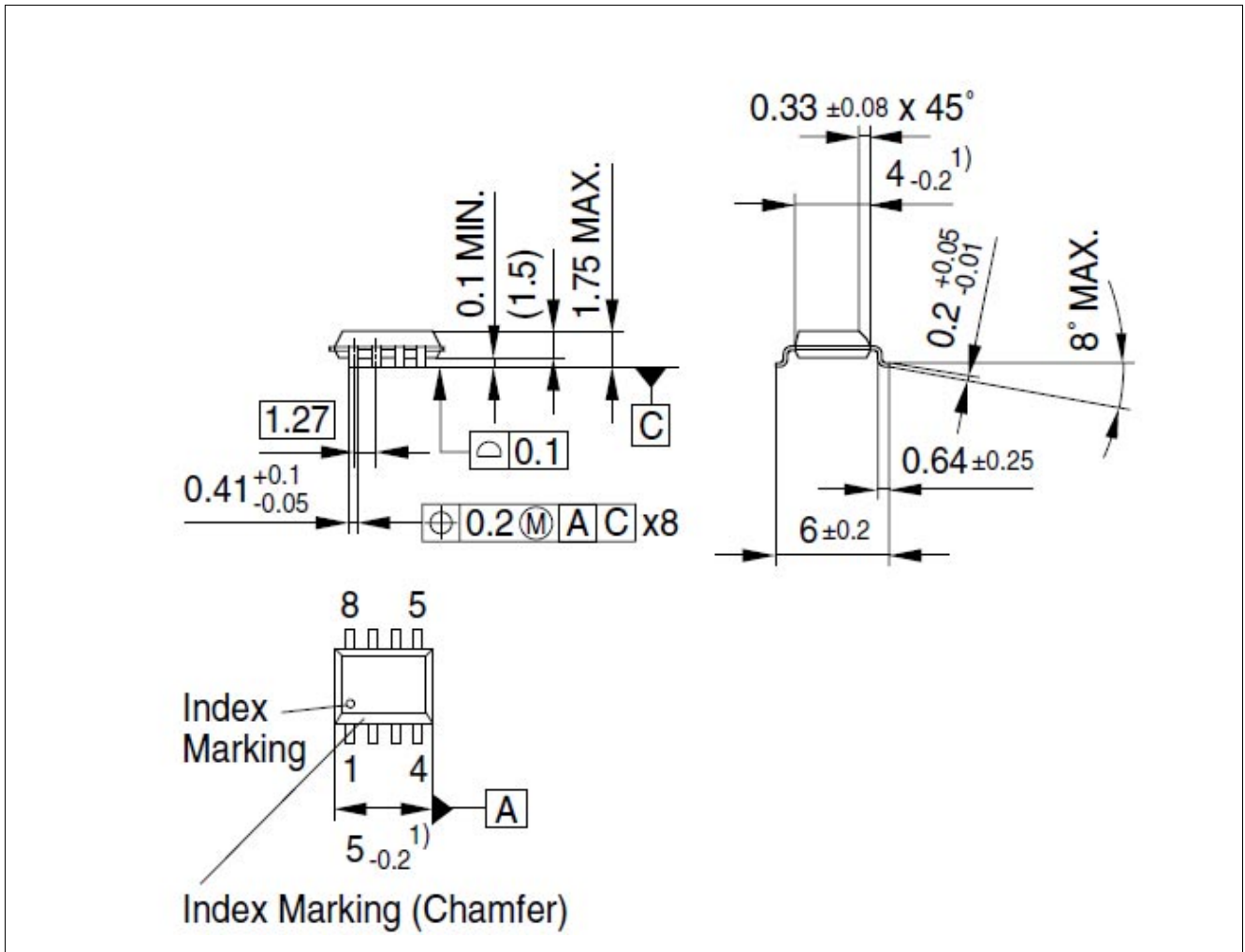


Figure 7 Protective behaviour of the ITS4100S-SJ-N

## 8 Package outlines and footprint



**Figure 8** PG-DSO-8 (Plastic Dual Small Outline Package, RoHS-Compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020

## 9 Revision History

Revision	Date	Changes
V 1.0	12-09-01	Datasheet release

### Trademarks of Infineon Technologies AG

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